

Dynamic quantum circuit compilation and circuit remapping

2310.11021 & PRApplied 22, 024029

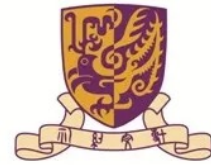
Kun Fang

School of Data Science

The Chinese University of Hong Kong, Shenzhen

Joint work with Yinan Li, Ruqi Shi, Munan Zhang, Di Yu

QCDAC2025@Shenzhen 2025.05.11



香港中文大學(深圳)
The Chinese University of Hong Kong, Shenzhen



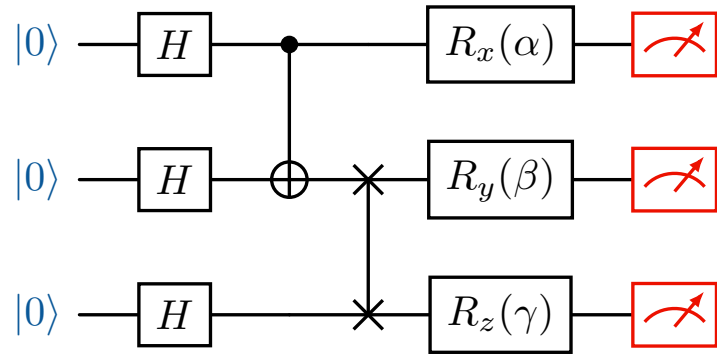
武漢大學
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THE UNIVERSITY OF HONG KONG

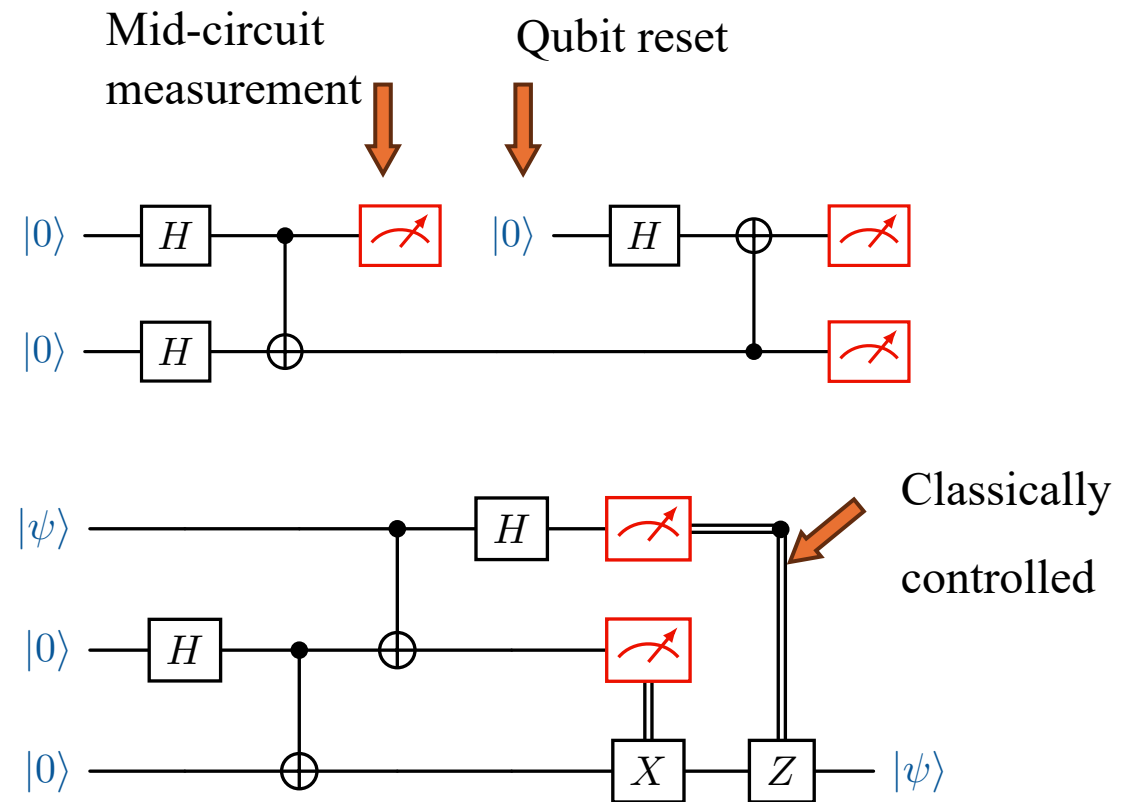
What is Dynamic Quantum Circuit

Static Quantum Circuit



- Start with state initialization
- Measurement at the end

Dynamic Quantum Circuit



Hardware Support for Dynamic Quantum Circuit

Exploiting Dynamic Quantum Circuits in a Quantum Algorithm with Superconducting Qubits

A. D. Córcoles, Maika Takita, Ken Inoue, Scott Lekuch, Zlatko K. Mineev, Jerry M. Chow, and Jay M. Gambetta
Phys. Rev. Lett. **127**, 100501 – Published 31 August 2021

IBM, 2021

Demonstration of the trapped-ion quantum CCD computer architecture

[J. M. Pino](#), [J. M. Dreiling](#), [C. Figgatt](#), [J. P. Gaebler](#), [S. A. Moses](#), [M. S. Allman](#), [C. H. Baldwin](#), [M. Foss-Feig](#), [D. Hayes](#) ✉, [K. Mayer](#), [C. Ryan-Anderson](#) & [B. Neyenhuis](#)

[Nature](#) **592**, 209–213 (2021) | [Cite this article](#)

Honeywell, 2021

Suppressing quantum errors by scaling a surface code logical qubit

[Google Quantum AI](#)

Superconducting Circuit

[Nature](#) **614**, 676–681 (2023) | [Cite this article](#)

Google, 2023

Midcircuit Qubit Measurement and Rearrangement in a ^{171}Yb Atomic Array

M. A. Norcia *et al.*

Phys. Rev. X **13**, 041034 (2023) – Published 22 November 2023

Atom Computing, 2023

Beating the break-even point with a discrete-variable-encoded logical qubit

[Zhongchu Ni](#), [Sai Li](#), [Xiaowei Deng](#), [Yanyan Cai](#), [Libo Zhang](#), [Weitong Wang](#), [Zhen-Biao Yang](#), [Haifeng Yu](#), [Fei Yan](#), [Song Liu](#), [Chang-Ling Zou](#), [Luyan Sun](#) ✉, [Shi-Biao Zheng](#) ✉, [Yuan Xu](#) ✉ & [Dapeng Yu](#) ✉

[Nature](#) **616**, 56–60 (2023) | [Cite this article](#)

SUSTech, 2023

Two benefits

Scalability

- Existing quantum computers are limited by the **number of qubits** available for computation. We need to **make efficient use of qubits** when designing and executing quantum algorithms.

Dynamic circuit can help to reduce the number of qubit use

Fidelity

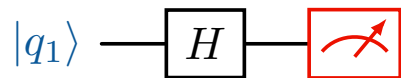
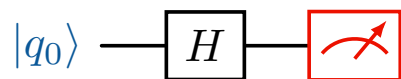
- Current generation of quantum computers are extremely prone to noise.
Circuit optimization and **error correction** needed !

Dynamic circuit can help to improve the circuit fidelity

What is dynamic circuit compilation

(yield same sampling results)

Rewires static quantum circuits into equivalent dynamic circuits using **fewer** qubits through qubit-reuse strategies.



What is dynamic circuit compilation

(yield same sampling results)

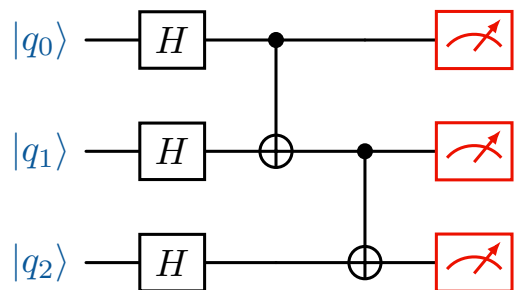
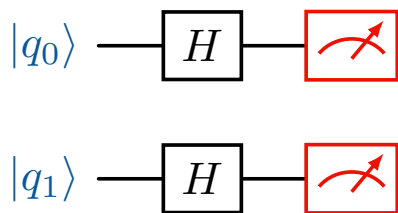
Rewires static quantum circuits into **equivalent** dynamic circuits using **fewer** qubits through **qubit-reuse** strategies.



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(yield same sampling results)

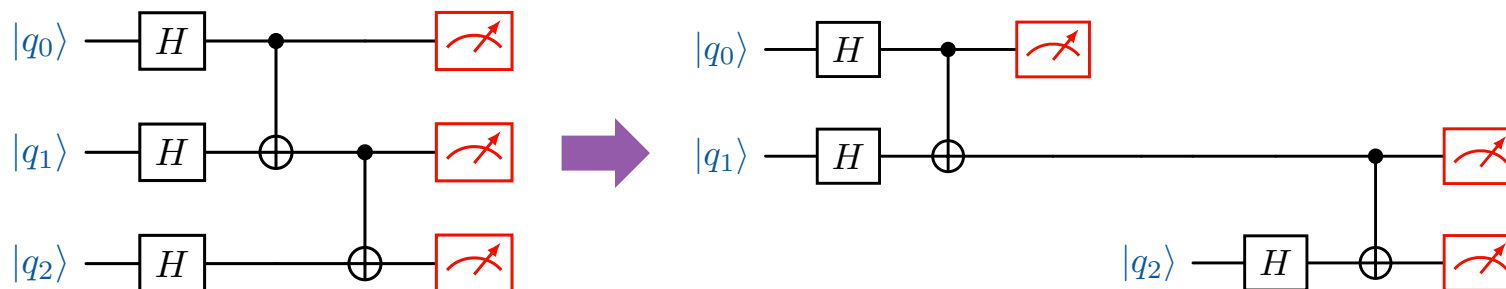
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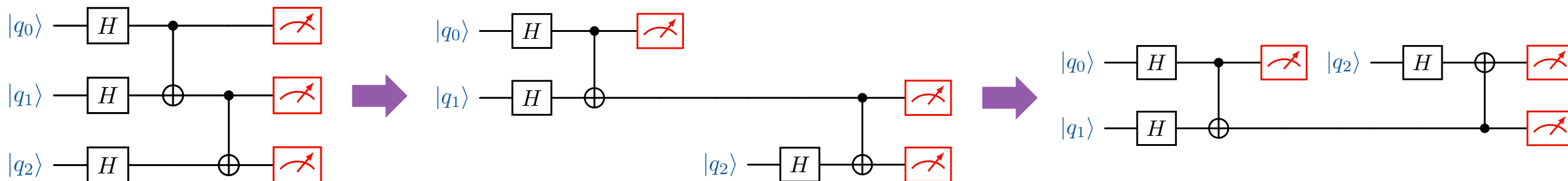
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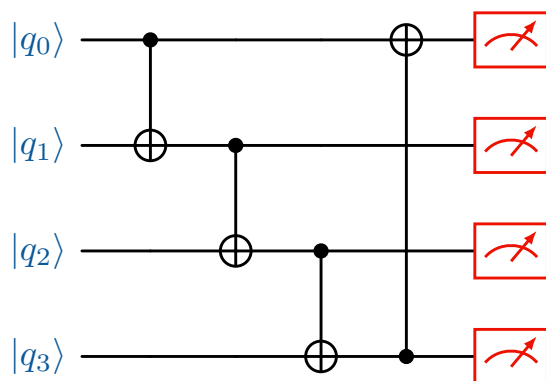
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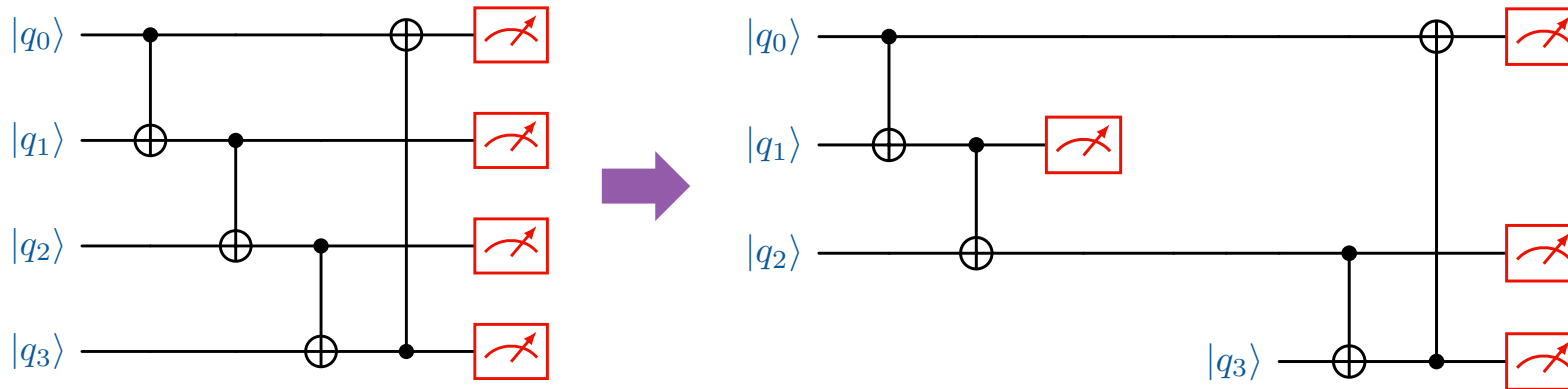
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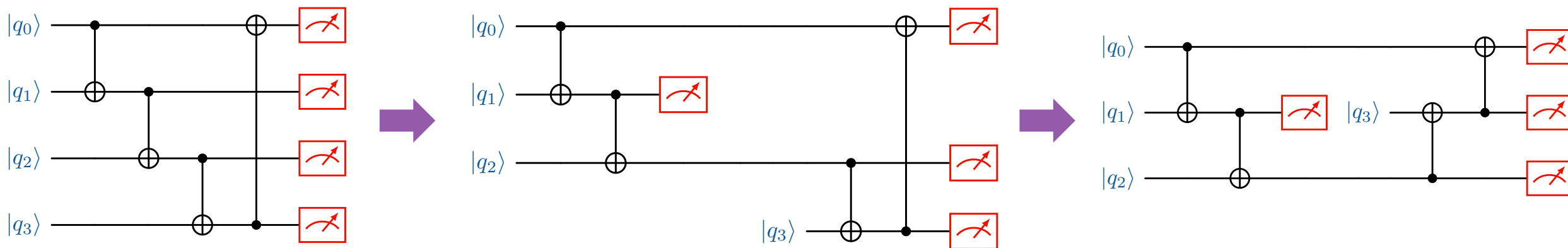
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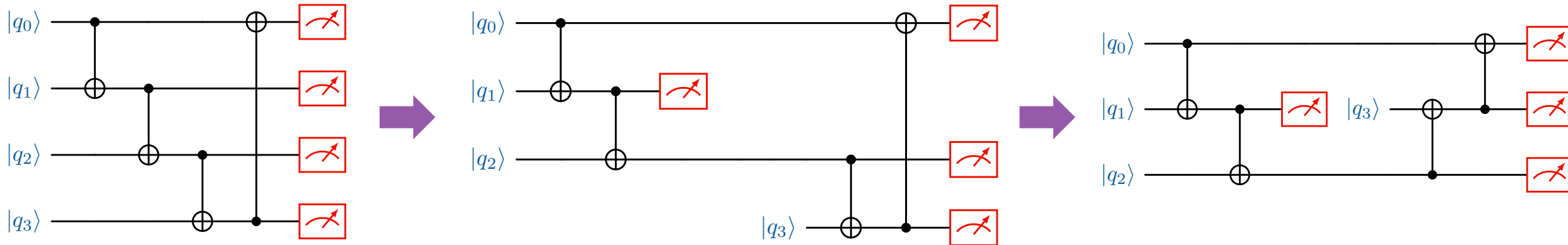
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using **fewer** qubits through qubit-reuse strategies.



What is dynamic circuit compilation

(yield same sampling results)

Rewires static quantum circuits into equivalent dynamic circuits using **fewer** qubits through qubit-reuse strategies.



Hard to compile manually for large circuits.

Automatic Tool Needed!

Take-home Message*

Large-Scale
Quantum Algorithm

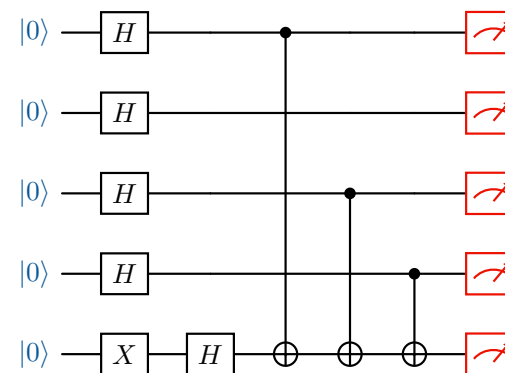
GAP

Quantum Computer
with Limited Resource

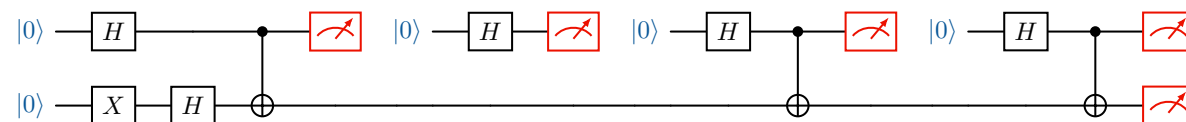
Dynamic
Quantum

Circuit
Compilation

N-qubit Bernstein-Vazirani Algorithm



2-qubit with Dynamic Circuit



Advantages

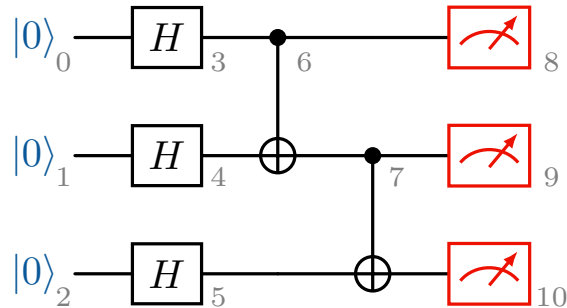
- **Qubit Saving**
- Swap Reduction
- Improved Fidelity

Circuit Compilation via Graph Manipulation*

From Circuit to Graph

Quantum Circuit Representations

Circuit Diagram

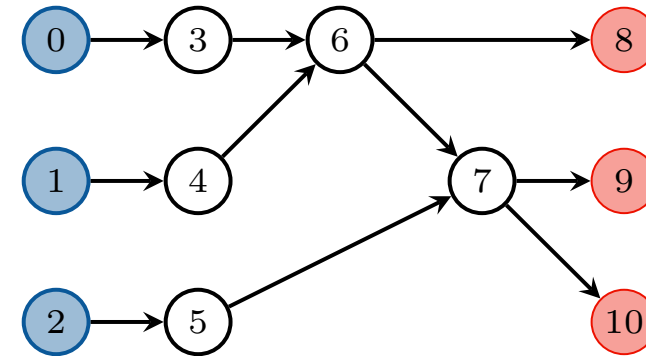


Circuit Instruction

Quantum Circuit Instructions

ID	TYPE	QUBIT	PAR
0	RESET	0	NONE
1	RESET	1	NONE
2	RESET	2	NONE
3	H	0	NONE
4	H	1	NONE
5	H	2	NONE
6	CX	[0, 1]	NONE
7	CX	[1, 2]	NONE
8	MEASURE	0	NONE
9	MEASURE	1	NONE
10	MEASURE	2	NONE

Directed Acyclic Graph (DAG) Representation

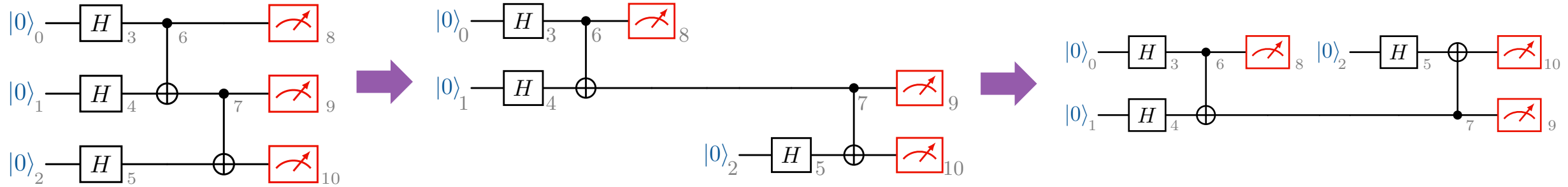


$$G(V = R \cup T \cup I, E)$$

- Root vertices ($r \in R$), indegree $\delta^-(r) = 0$
- Terminal vertices ($t \in T$), outdegree $\delta^+(t) = 0$
- Internal vertices ($i \in I$), $\delta^-(i) \neq 0, \delta^+(i) \neq 0$

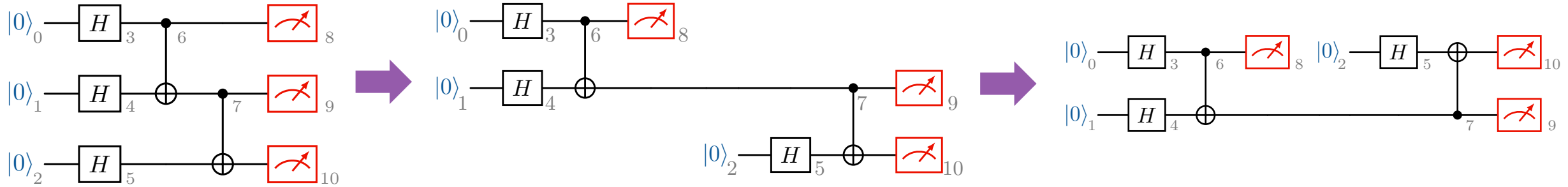
Quantum Circuit Compilation via Graph Manipulation*

Dynamic Circuit Compilation

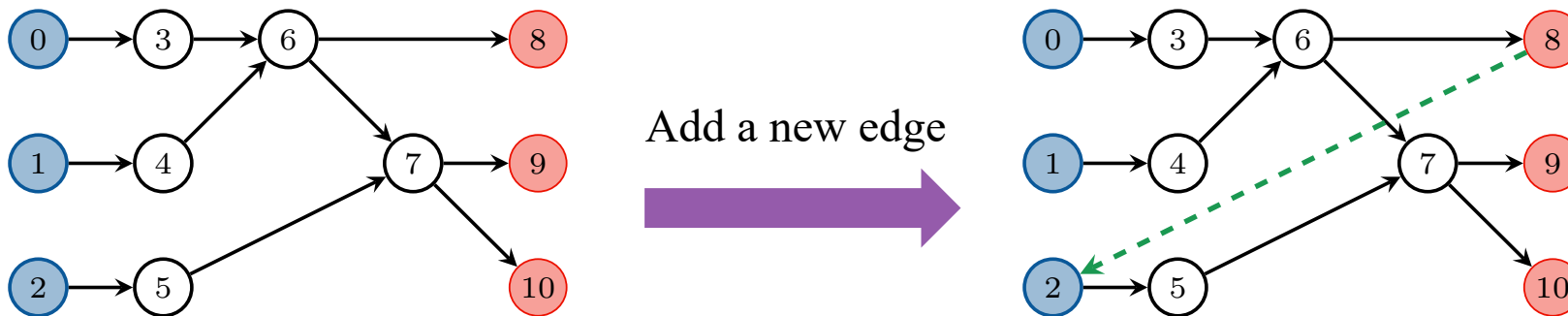


Quantum Circuit Compilation via Graph Manipulation*

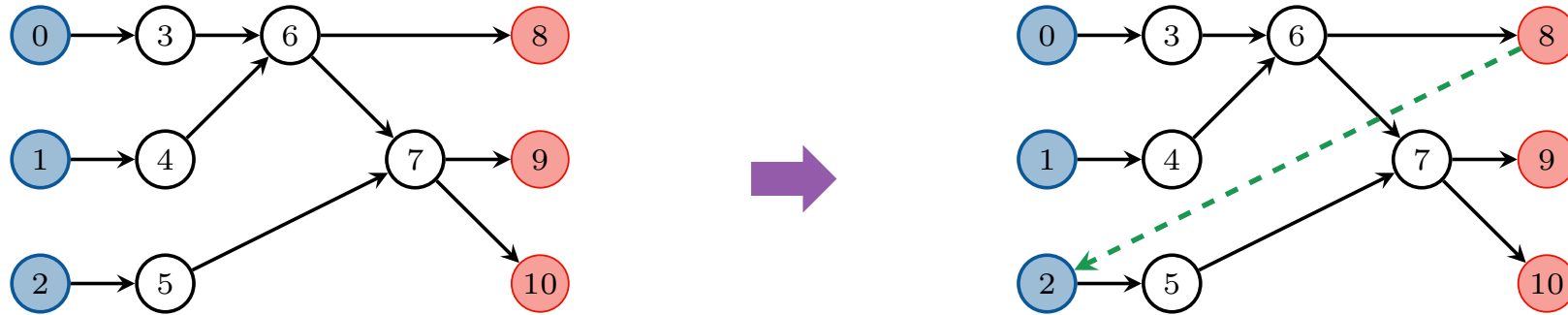
Dynamic Circuit Compilation



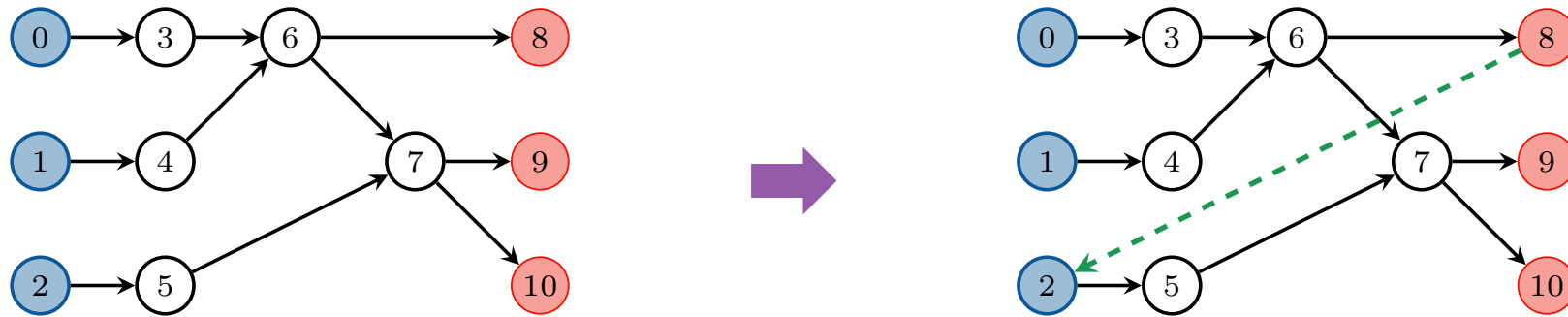
Graph Manipulation



Quantum Circuit Compilation via Graph Manipulation*



Quantum Circuit Compilation via Graph Manipulation*



- $\forall (t, r) \in E', \text{ it has } t \in T \text{ and } r \in R;$

Constraints

- $\forall (t, r) \in E', \text{ it has } \text{outdegree}(t) = 1 \text{ and } \text{indegree}(r) = 1;$
- $G' = (R \cup T, E \cup E')$ is an **acyclic** graph.

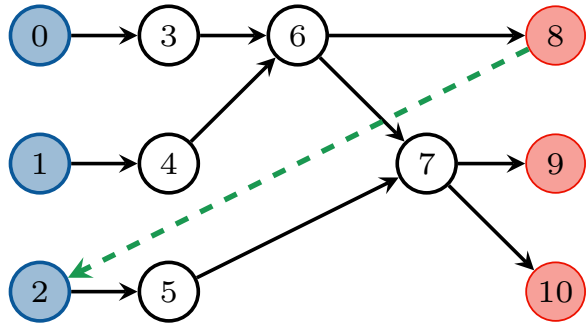
To ensure that the graph manipulation corresponds to a valid circuit compilation

Circuit Compilation via Graph Manipulation*

From Graph to Circuit

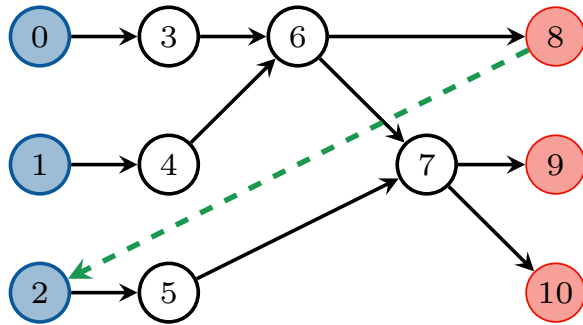
Quantum Circuit Compilation via Graph Manipulation*

DAG with new edges



Quantum Circuit Compilation via Graph Manipulation*

DAG with new edges



Topological



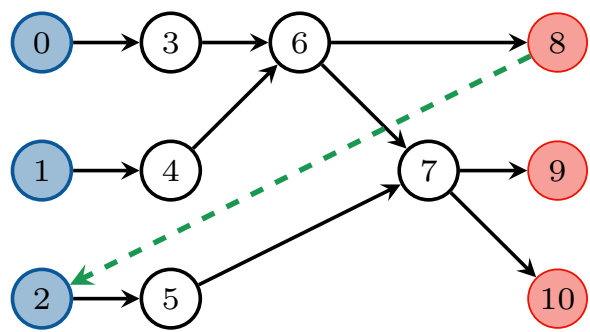
Ordering

Feasible Execution Sequence

0 → 1 → 3 → 4 → 6 → 8 → 2 → 5 → 7 → 10 → 9

Quantum Circuit Compilation via Graph Manipulation*

DAG with new edges



Topological



Ordering

every directed path from u to v ,
 u comes before v in the ordering

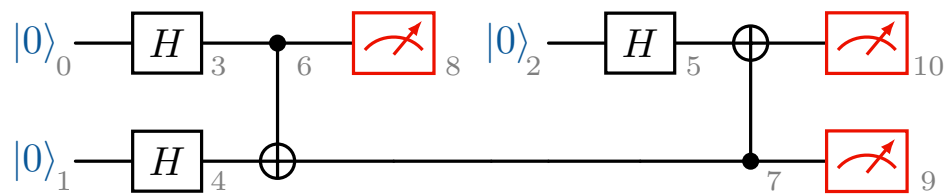
Feasible Execution Sequence

$0 \rightarrow 1 \rightarrow 3 \rightarrow 4 \rightarrow 6 \rightarrow 8 \rightarrow 2 \rightarrow 5 \rightarrow 7 \rightarrow 10 \rightarrow 9$

Qubit ↓ **Reallocation**

Dynamic Circuit Instructions

Dynamic Circuit

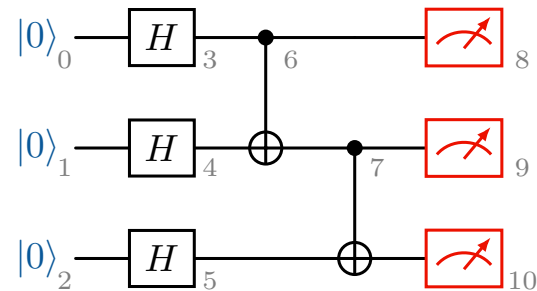


Quantum Circuit Instructions			
ID	TYPE	QUBIT	PAR
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1	RESET	1	NONE
3	H	0	NONE
4	H	1	NONE
6	CX	[0, 1]	NONE
8	MEASURE	0	NONE
2	RESET	0	NONE
5	H	0	NONE
7	CX	[1, 0]	NONE
10	MEASURE	0	NONE
9	MEASURE	1	NONE

Reallocate 2 to 0

Compilation Procedures

Static Circuit

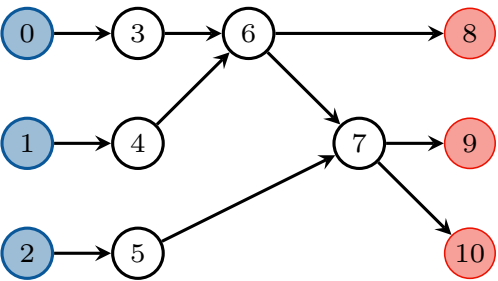


Input Circuit

Static Circuit Instruction

Quantum Circuit Instructions			
ID	TYPE	QUBIT	PAR
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1	RESET	1	NONE
2	RESET	2	NONE
3	H	0	NONE
4	H	1	NONE
5	H	2	NONE
6	CX	[0, 1]	NONE
7	CX	[1, 2]	NONE
8	MEASURE	0	NONE
9	MEASURE	1	NONE
10	MEASURE	2	NONE

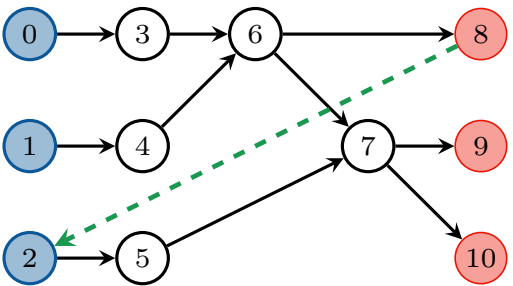
DAG Representation



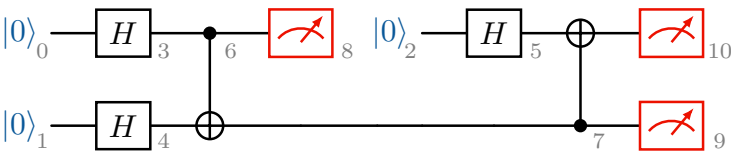
Dynamic Circuit Instruction

Quantum Circuit Instructions			
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8	MEASURE	0	NONE
2	RESET	0	NONE
5	H	0	NONE
7	CX	[1, 0]	NONE
10	MEASURE	0	NONE
9	MEASURE	1	NONE

DAG with a new edge



Dynamic Circuit



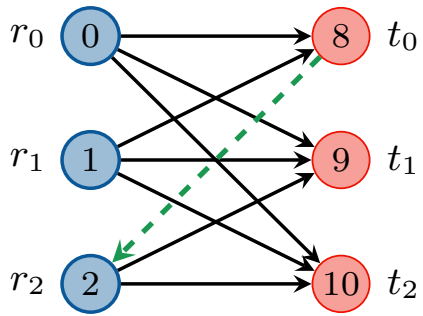
Output Circuit

Optimal Circuit Compilation for Maximizing Qubit Reuse

Optimal Circuit Compilation for Maximizing Qubit Reuse

Optimal Quantum Circuit Compilation as a Binary Integer Programming Problem

Simplified DAG



Biadjacency Matrix

$$\begin{matrix} & t_0 & t_1 & t_2 \\ \begin{matrix} r_0 \\ r_1 \\ r_2 \end{matrix} & \begin{pmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 0 & 1 & 1 \end{pmatrix} \end{matrix}$$

Candidate Matrix

$$\begin{matrix} & r_0 & r_1 & r_2 \\ \begin{matrix} t_0 \\ t_1 \\ t_2 \end{matrix} & \begin{pmatrix} 0 & 0 & 1 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} \end{matrix}$$

Graph Manipulation

- $\forall (t, r) \in E'$, it has $t \in T$ and $r \in R$;
- $\forall (t, r) \in E'$, it has $\text{outdegree}(t) = 1$ and $\text{indegree}(r) = 1$;
- $G' = (R \cup T, E \cup E')$ is an acyclic graph.

Exact Characterization

$$\alpha := \max \sum_{i,j=0}^{n-1} F_{ij} \quad \text{Maximized added edges}$$

$$\text{s. t. } F_{ij} \leq \bar{B}_{ij}, \forall i, j \in \{0, 1, \dots, n-1\}$$

$$\sum_{j=0}^{n-1} F_{ij} \leq 1, \forall i \in \{0, 1, \dots, n-1\}$$

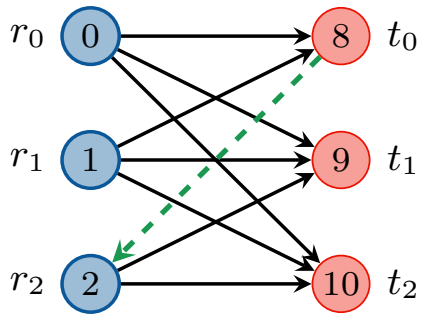
$$\sum_{i=0}^{n-1} F_{ij} \leq 1, \forall j \in \{0, 1, \dots, n-1\}$$

$$\begin{pmatrix} O_n & B \\ F & O_n \end{pmatrix} \quad \text{nilpotent}$$

Optimal Circuit Compilation for Maximizing Qubit Reuse

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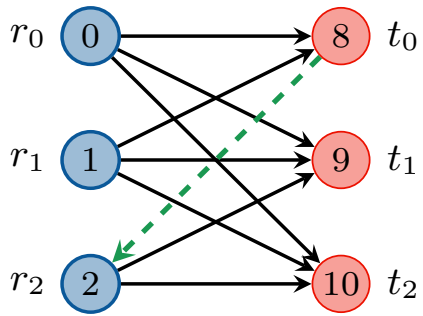
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Optimal Circuit Compilation for Maximizing Qubit Reuse

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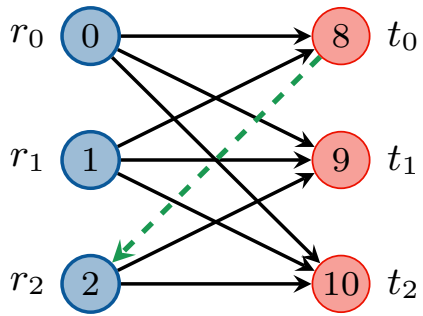
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Optimal Circuit Compilation for Maximizing Qubit Reuse

Optimal Quantum Circuit Compilation as a Binary Integer Programming Problem

Simplified DAG



Biadjacency Matrix

$$r_0 \begin{pmatrix} t_0 & t_1 & t_2 \\ 1 & 1 & 1 \end{pmatrix}$$

$$r_1 \begin{pmatrix} 1 & 1 & 1 \end{pmatrix}$$

$$r_2 \begin{pmatrix} 0 & 1 & 1 \end{pmatrix}$$

Candidate Matrix

$$t_0 \begin{pmatrix} r_0 & r_1 & r_2 \\ 0 & 0 & 1 \end{pmatrix}$$

$$t_1 \begin{pmatrix} 0 & 0 & 0 \end{pmatrix}$$

$$t_2 \begin{pmatrix} 0 & 0 & 0 \end{pmatrix}$$

Exact Characterization

$$\alpha := \max \sum_{i,j=0}^{n-1} F_{ij} \quad \text{Maximized added edges}$$

$$\text{s.t. } F_{ij} \leq \bar{B}_{ij}, \forall i, j \in \{0, 1, \dots, n-1\}$$

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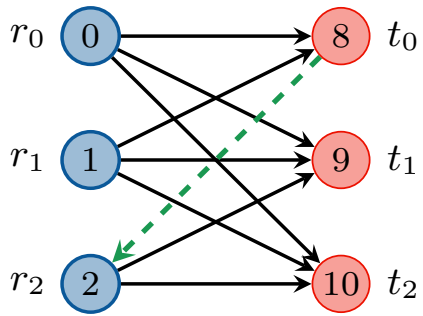
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- $G' = (R \cup T, E \cup E') \text{ is an acyclic graph.}$

Exact Characterization

$$\begin{aligned} \alpha &:= \max \sum_{i,j=0}^{n-1} F_{ij} && \textbf{NP-hard}^{[*]} \\ \text{s. t. } &F_{ij} \leq \bar{B}_{ij}, \forall i, j \in \{0, 1, \dots, n-1\} \\ &\begin{cases} \sum_{j=0}^{n-1} F_{ij} \leq 1, \forall i \in \{0, 1, \dots, n-1\} \\ \sum_{i=0}^{n-1} F_{ij} \leq 1, \forall j \in \{0, 1, \dots, n-1\} \end{cases} \\ &\begin{pmatrix} O_n & B \\ F & O_n \end{pmatrix} \text{ nilpotent} \end{aligned}$$

[1] Hanru Jiang. 2024. Qubit Recycling Revisited. Proc. ACM Program. Lang. 8, PLDI, Article 198 (June 2024), 24 pages.

[*] The author in [1] proved that an equivalent optimization problem is NP-hard.

Optimal Circuit Compilation for Maximizing Qubit Reuse

Summary of Explored Circuits

Quantum circuits	Original	Compiled
Bernstein-Vazirani algorithm	$n + 1$	2 (1)
* Quantum Fourier transform	n	n
* Quantum phase estimation	n	n
* Shor's algorithm	n	n
Grover's algorithm	n	n
Quantum counting algorithm	n	n
Quantum ripple carry adder circuit	n (4)	4 (3)
Linearly entangled circuit with l layers	n	$l + 1$
Circularly entangled circuit with l layers	n	3
Pairwisely entangled circuit with l layers	n	$2l + 1$
Fully entangled circuit	n	n
Diamond-structured quantum circuit	$2n$	$n + 1$
MBQC with cluster state of size (w, d)	wd	$w + 1$
MBQC with brickwork state of size (w, d)	wd	$w + 1$

Cases in red indicates the compiled width is **optimal** and cases in blue indicates **irreducible circuit**.

* **Depends on specific circuit implementation of the algorithm**

Refer to the full paper for more details [arXiv: 2310.1102]

Heuristic Algorithms

How to add as many edges as possible?

Heuristic Algorithm: Greedy Algorithms*

Algorithm: Greedy Algorithm

Greedy Algorithm

Makes a **locally optimal** choice at each step



Maximize the possibility to add more edges in subsequent steps

Heuristic Algorithm: Greedy Algorithms*

Algorithm: Greedy Algorithm

Greedy Algorithm

Makes a **locally optimal** choice at each step



Maximize the possibility to add more edges in subsequent steps

Procedure

- **Temporarily** integrates the edge into the simplified DAG and update the candidate matrix
- Score the candidate edge as the **summation** of all elements within the updated candidate matrix
- **Randomly** select a candidate edge with the **highest score**

Heuristic Algorithm: Greedy Algorithms*

Algorithm: Greedy Algorithm

Worst-case Time Complexity $O(mn + n^5)$

n: input circuit width, m: # of instructions

e.g. 5-qubit Bernstein-Vazirani

Edge under evaluation

0	1	1	1	0
1	0	1	1	1
0	1	0	1	0
0	1	0	0	0
0	1	0	0	0

Update candidate matrix

0	1	1	1	0
0	0	0	0	0
0	1	0	1	0
0	1	0	0	0
0	1	0	0	0

0	0	1	1	0
0	0	0	0	0
0	0	0	1	0
0	0	0	0	0
0	0	0	0	0

Score matrix

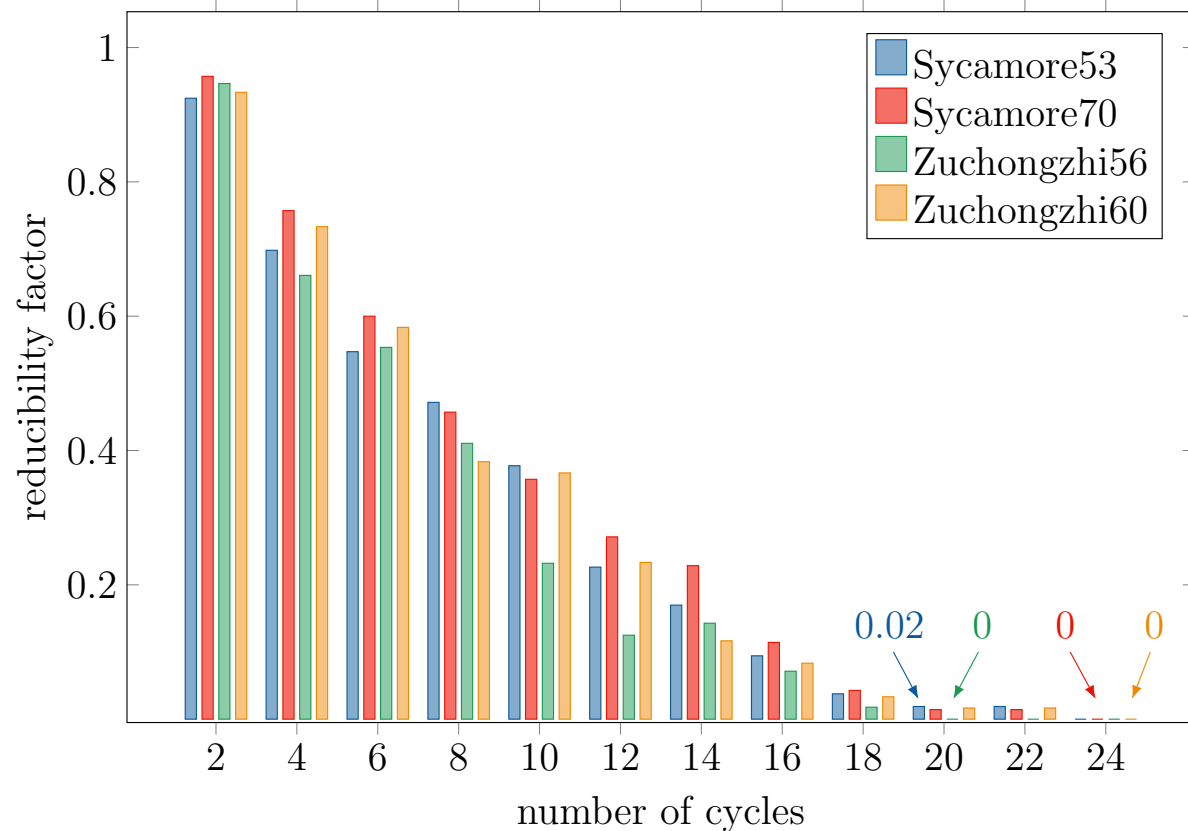
0	3	7	6	0
3	0	3	3	3
0	3	0	7	0
0	3	0	0	0
0	3	0	0	0

Numerical Evaluation

Performance of the heuristic algorithms?

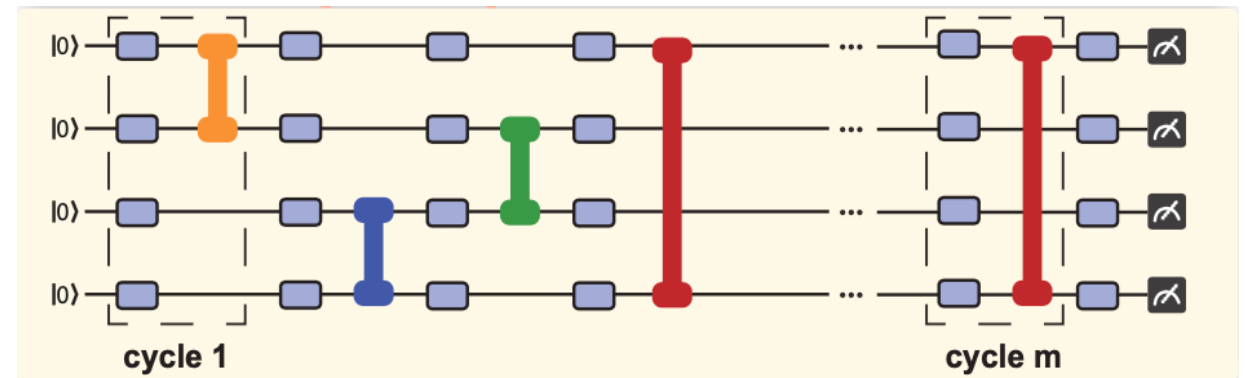
Numerical Evaluation: Quantum Supremacy Circuits

*Demonstrating Quantum Supremacy



Reducibility Factor $r = 1 - \frac{\text{compiled width}}{\text{original width}} \in [0, 1)$

The larger, the better



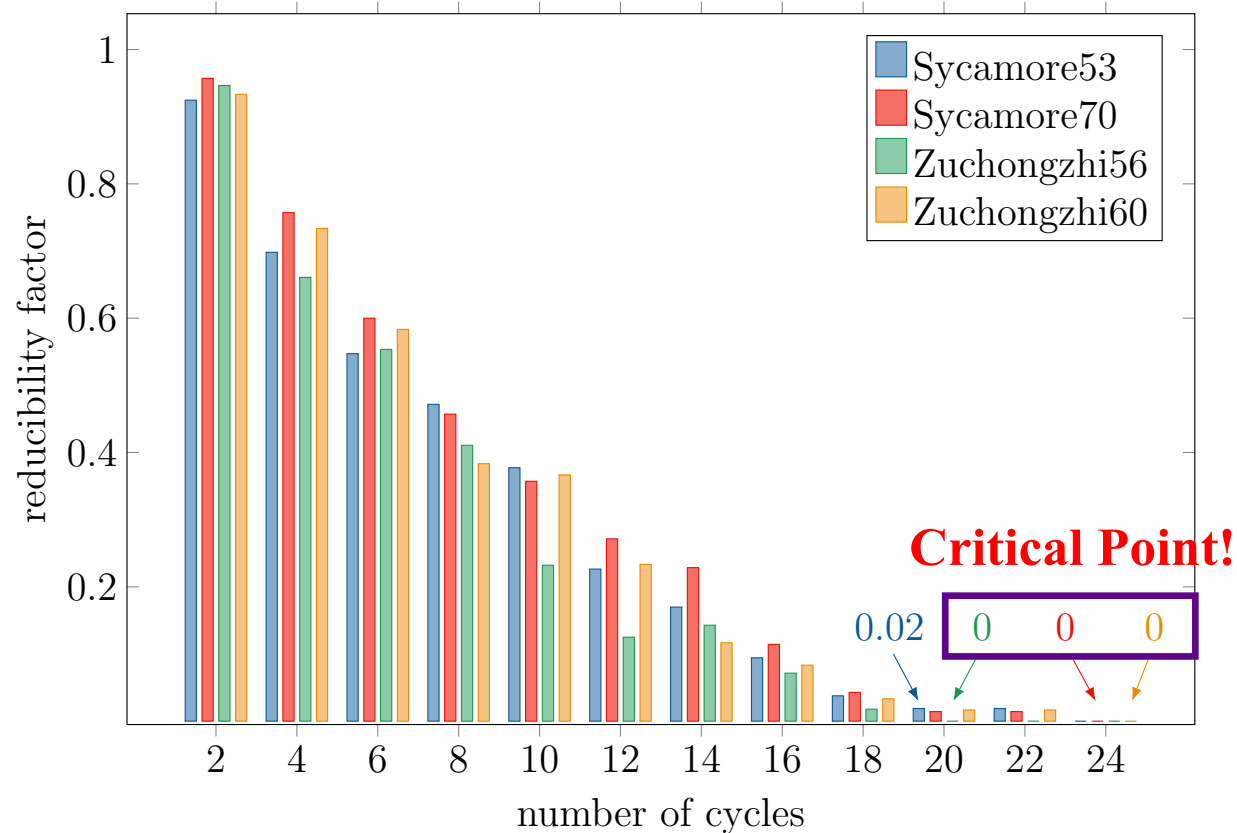
The number of cycles cannot be too large or too small.

How to determine this number?

- [1] Frank Arute et al. Quantum supremacy using a programmable superconducting processor. *Nature* 574, 505-510 (2019).
- [2] Alexis Morvan et al. Phase transition in Random Circuit Sampling. arXiv:2304.11119 (2023).
- [3] Yulin Wu et al. Strong quantum computational advantage using a superconducting quantum processor. *Phys. Rev. Lett.* 127, 180501 (2021).
- [4] Qingling Zhu et al. Quantum computational advantage via 60-qubit 24-cycle random circuit sampling. *Science Bulletin* 67, 240-245 (2022).

Numerical Evaluation: Quantum Supremacy Circuits

*Demonstrating Quantum Supremacy



Interesting Observation I

Sycamore 70

Zuchongzhi 56

Zuchongzhi 60



Irreducible
Quantum Circuit

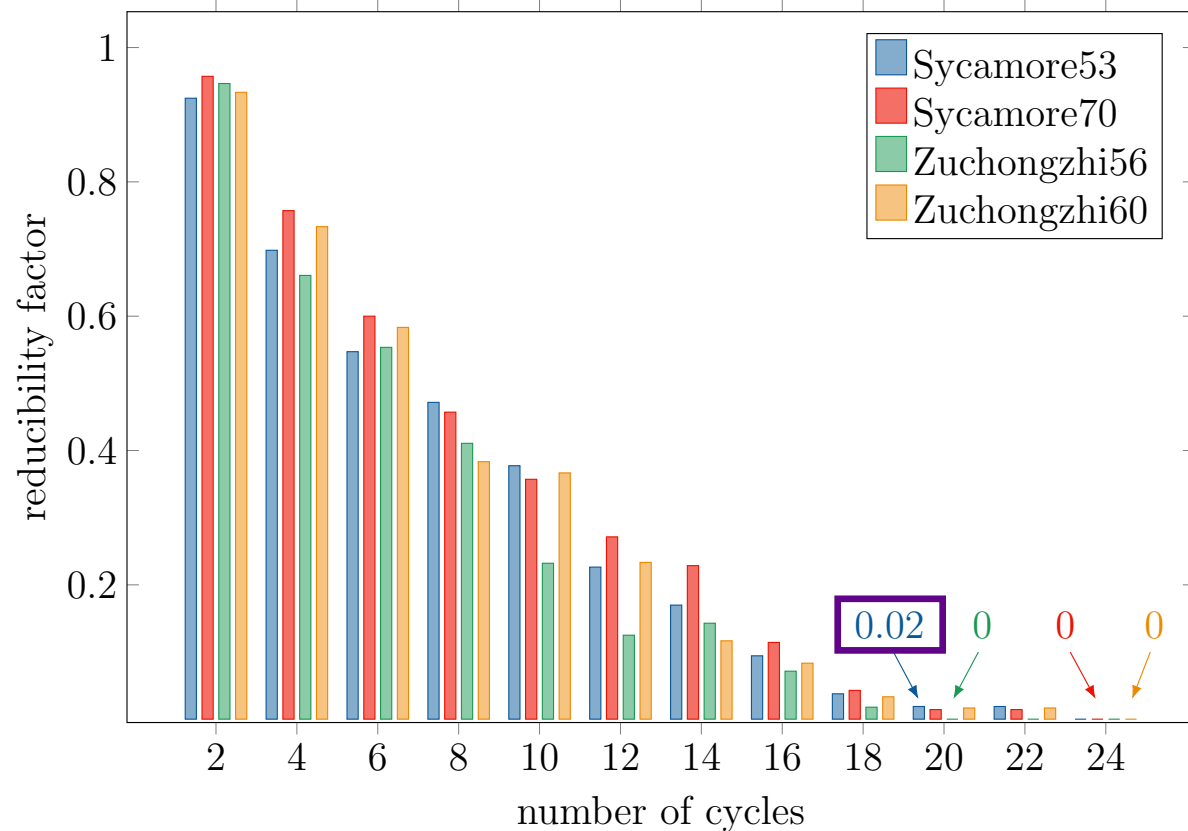
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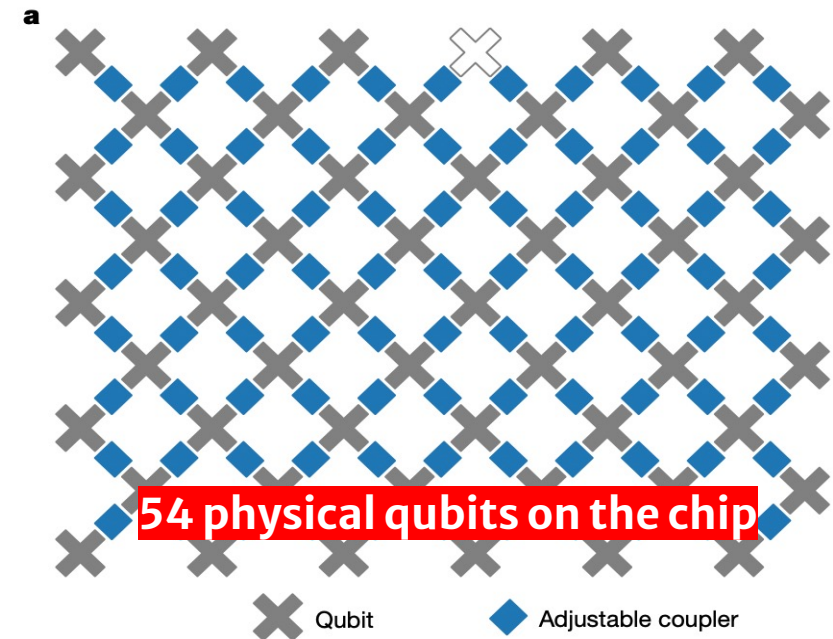
Numerical Evaluation: Quantum Supremacy Circuits

*Demonstrating Quantum Supremacy



Interesting Observation II

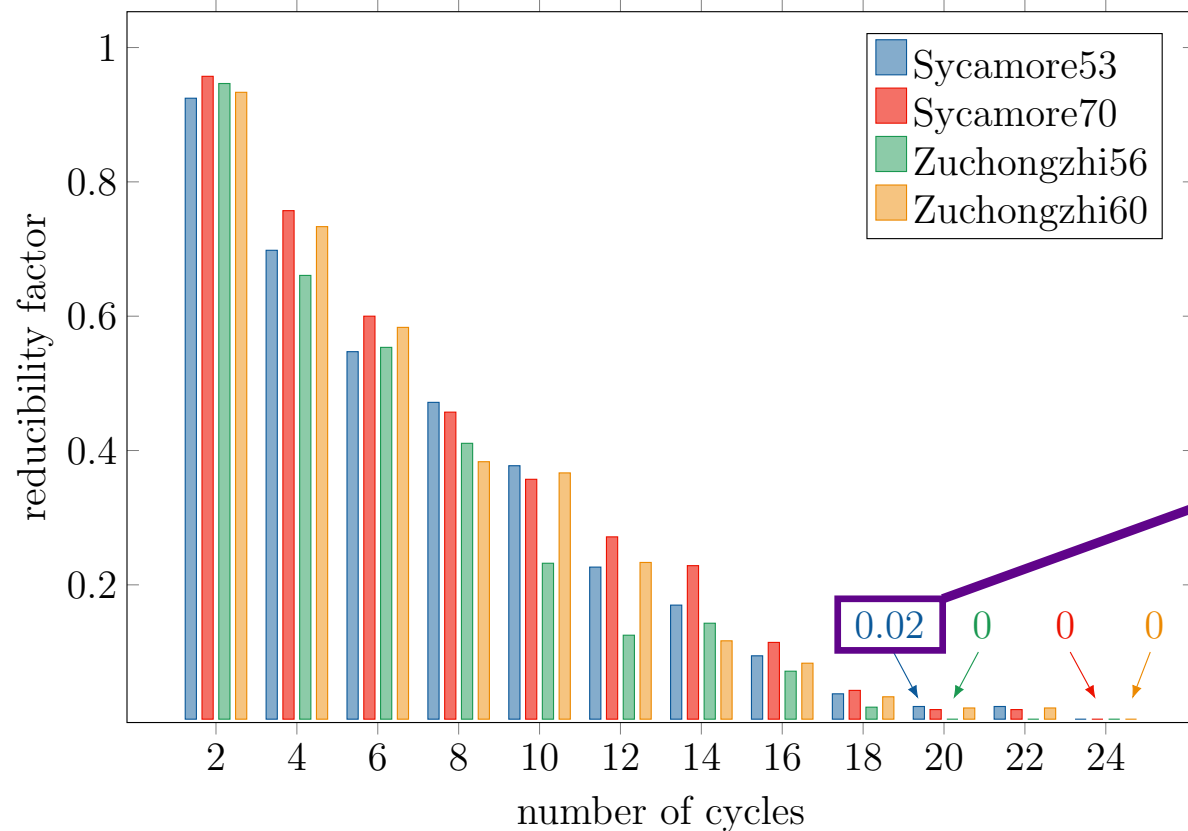
Sycamore 53 $\rightarrow r = 0.02$



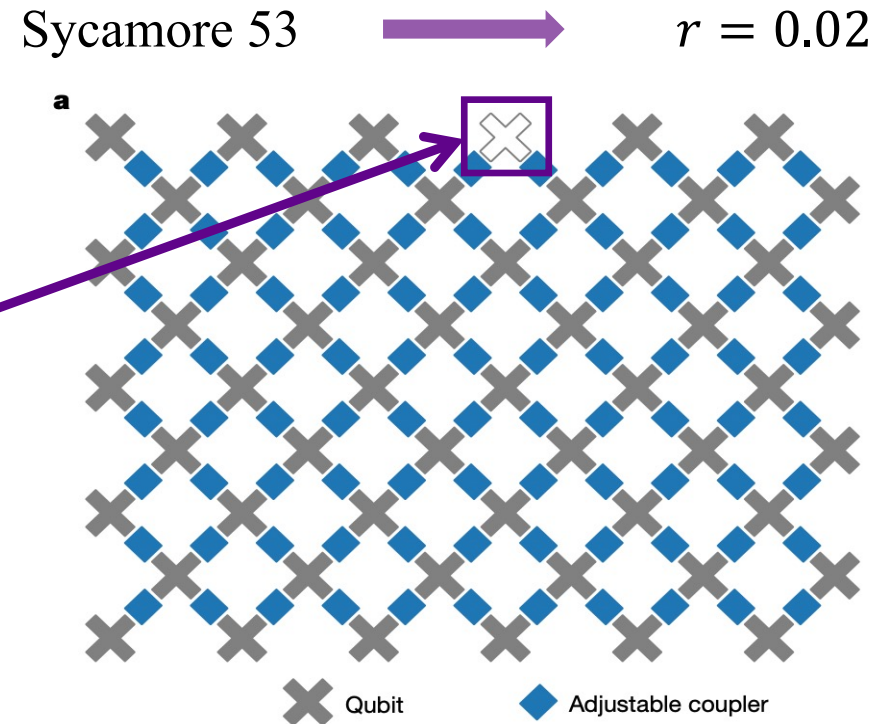
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Numerical Evaluation: Quantum Supremacy Circuits

*Demonstrating Quantum Supremacy



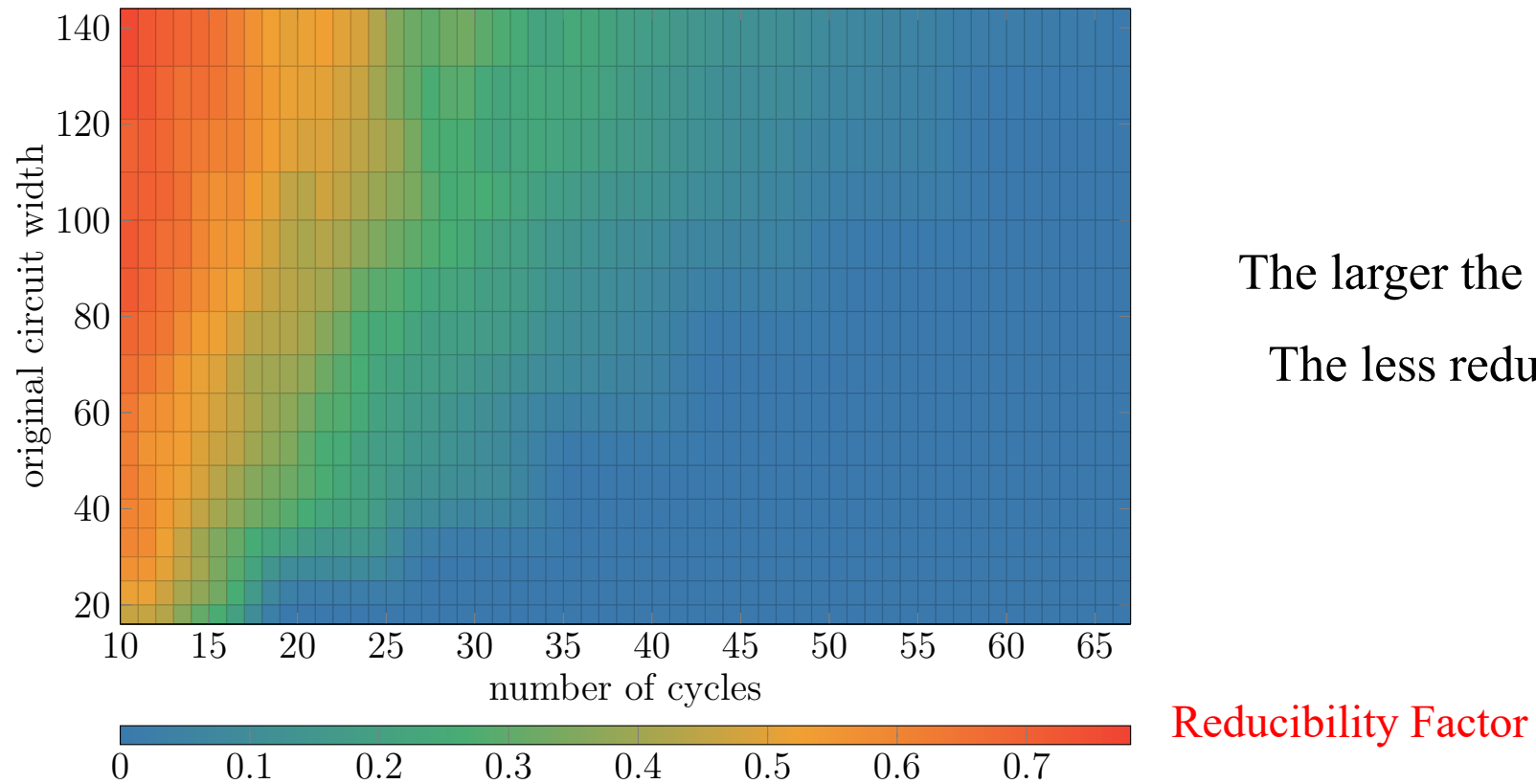
Interesting Observation II



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Numerical Evaluation: Quantum Supremacy Circuits

Google Random Circuit Sampling (GRCS)



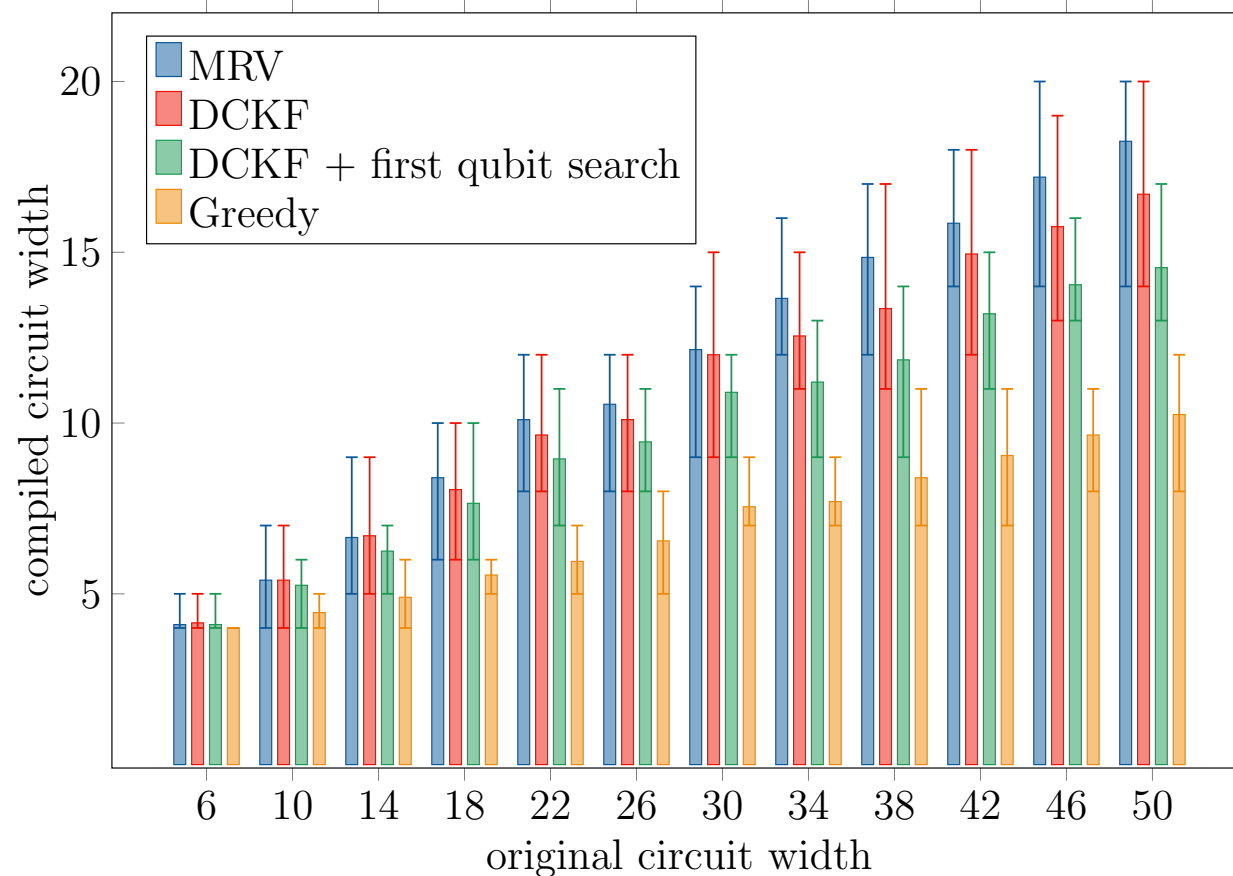
[1] Sergio Boixo et al. Characterizing quantum supremacy in near-term devices. *Nature Phys* **14**, 595–600 (2018).

[2] GRCS. <https://github.com/sboixo/GRCS>

Numerical Evaluation: QAOA circuits

QAOA circuits for max-cut problem on random 3-regular graph

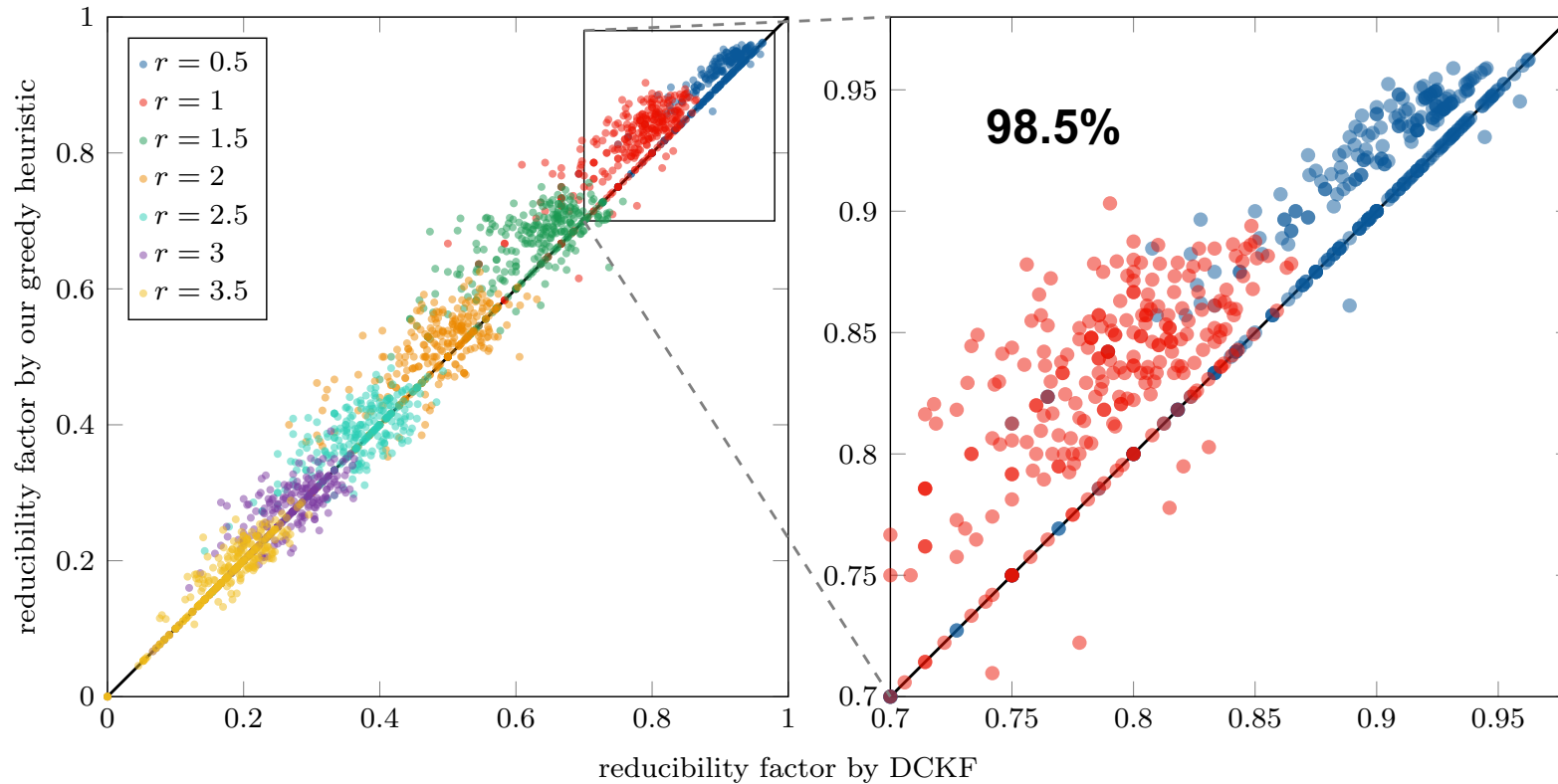
Commutable ZZ gates



Our methods account for **commutable gates**, which leads to better performance.

Numerical Evaluation: Random Quantum Circuits

Normal Random Circuit

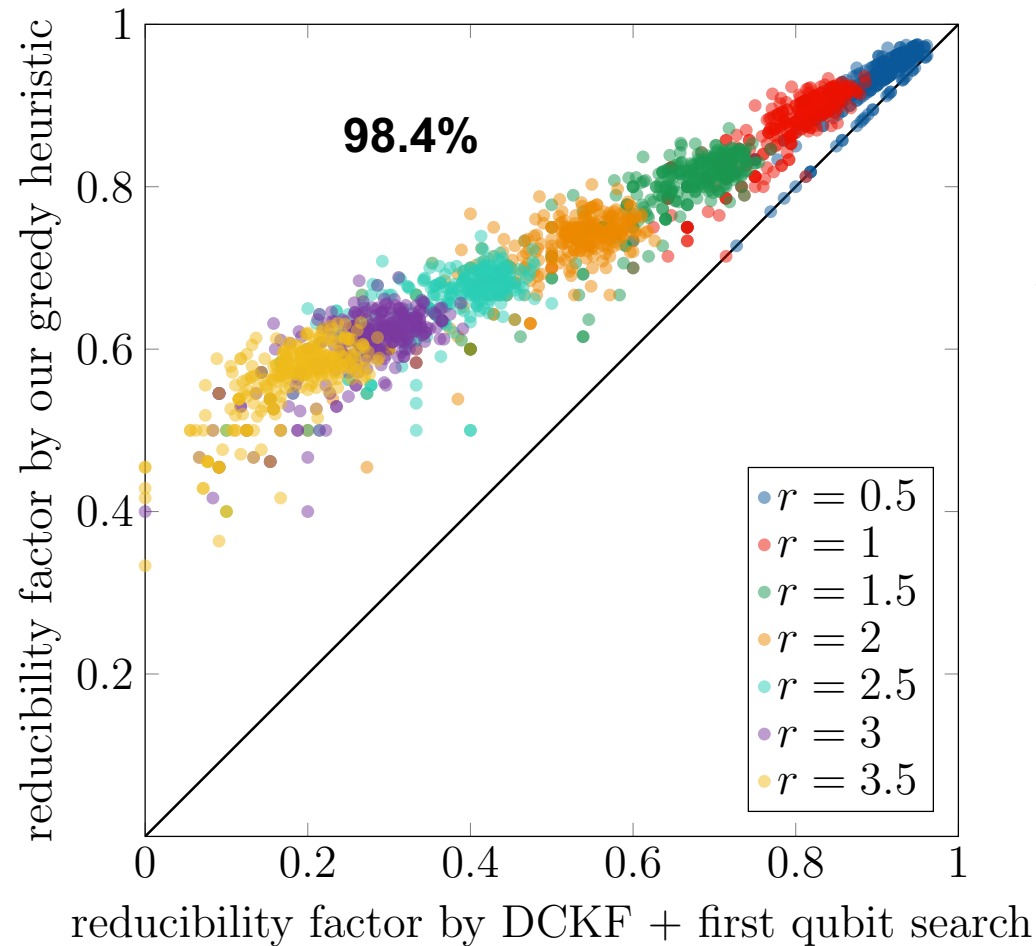


$$r = \frac{\# \text{ of two-qubit gates}}{\# \text{ of qubits}}$$

Outperforms in approximately **87.6%**
of cases, with a **strict advantage** over
49.6% of random circuits

Numerical Evaluation: Random Quantum Circuits

Random IQP Circuit



A lot of commutable gates

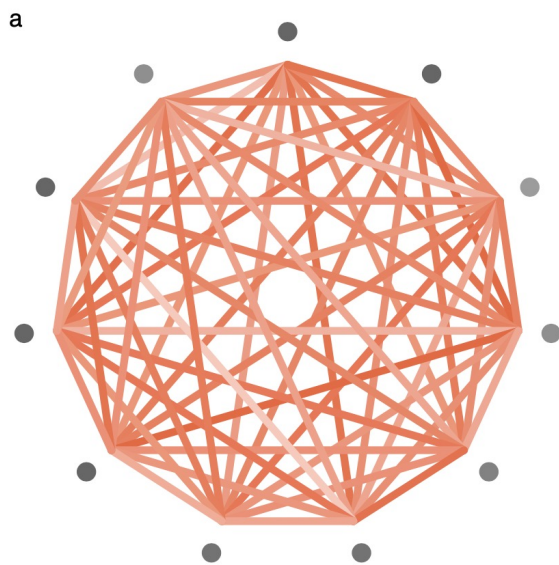
**Outperforms in nearly
100% of instances**

Numerical Evaluation: Noisy Simulation

Noisy Simulation of a 11-qubit Bernstein-Vazirani Algorithm

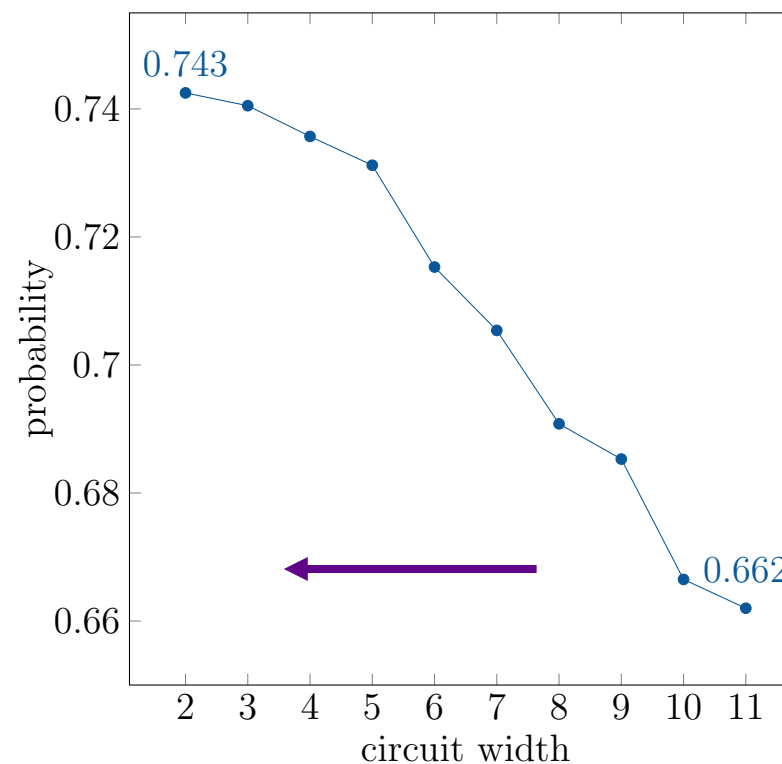
Compilation reduces the number of qubits required,
allowing us to choose physical qubits with better performance.

11-qubit Trapped-Ion Quantum Computer^[1]



All-to-all connectivity

Experiment Results

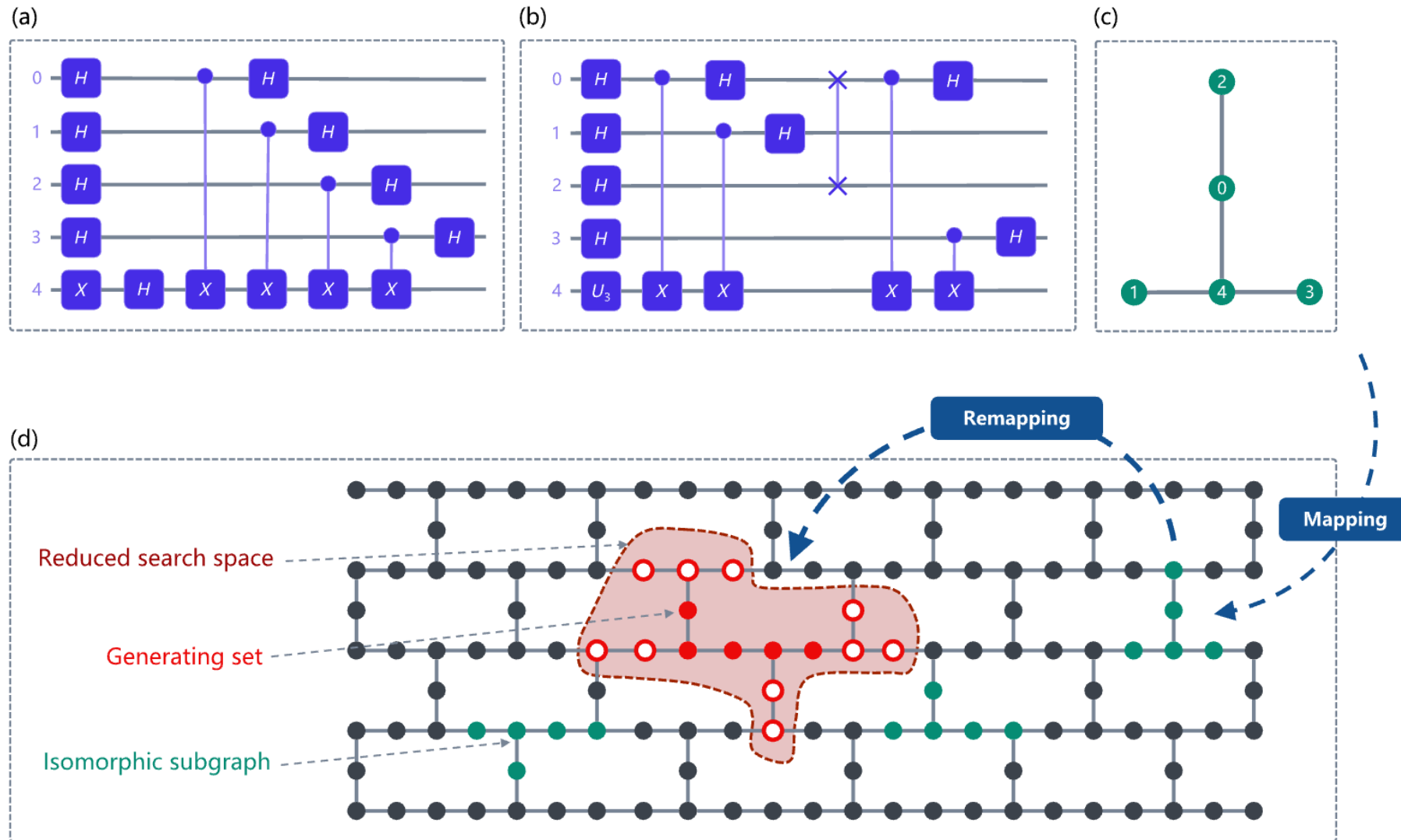


Qubit reduce up to 82% and probability improve 9%

[1] K. Wright et al. Benchmarking an 11-qubit quantum computer. *Nature Communications* 10, 5464 (2019).

Quantum circuit remapping using symmetry

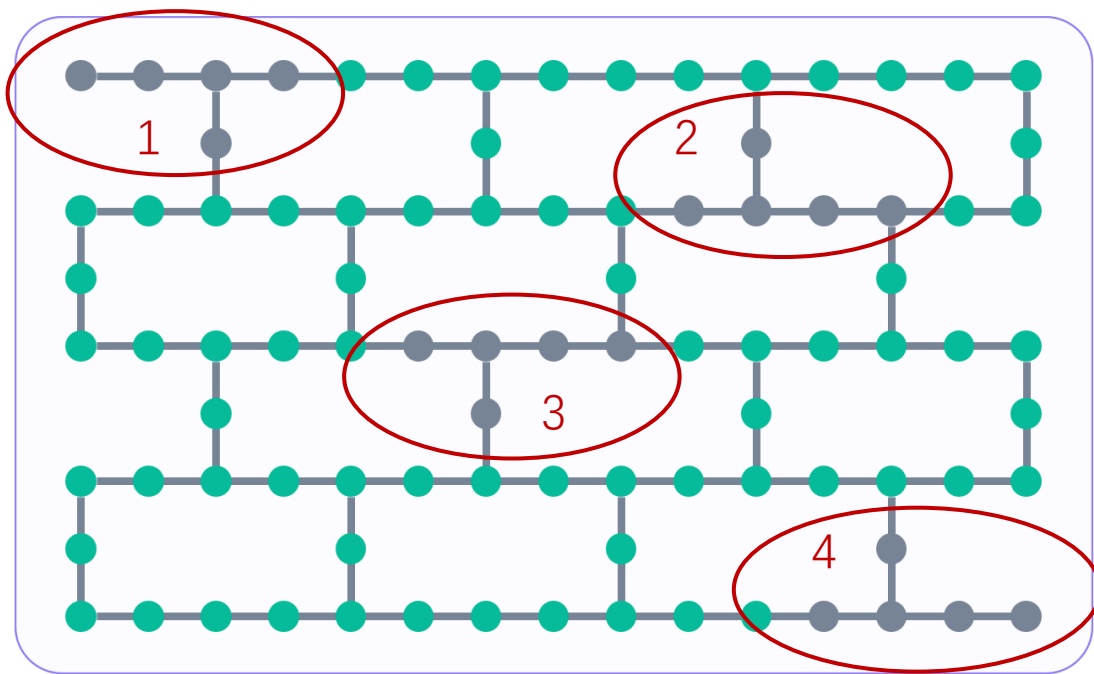
Quantum circuit mapping and remapping



Qubit mapping: determine which **physical qubits** will be used for executing a **logical quantum circuit**.

Subgraph Matching Problem

- In a real quantum system, each qubit has different performance, some good and some bad.
- **How to find the best set of qubits to implement your circuit?**
- Find all isomorphic graphs



Coupling graph of a quantum chip

Subgraph matching problem

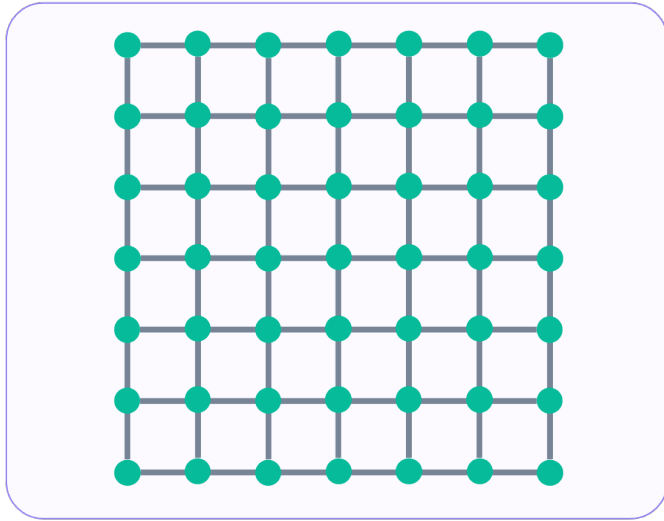
Given a graph G and a graph T , what are all subgraphs in G that are isomorphic to T ?

(Stephen A. Cook, 1971) Subgraph matching problem is **NP-complete in general**.

But the **good news** is that the coupling graph is **symmetric**

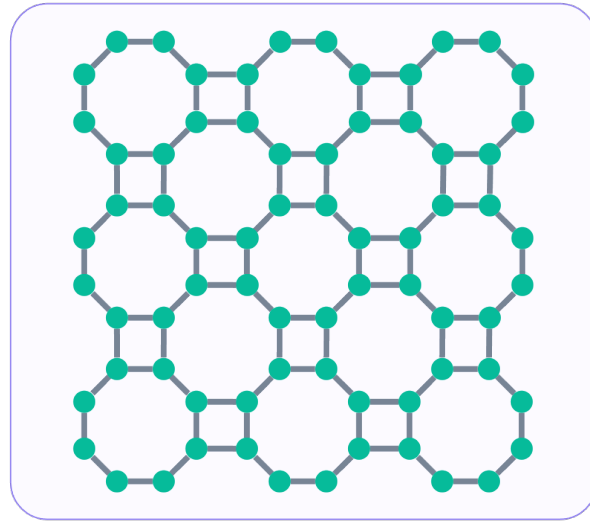
Common quantum hardware structures and their symmetries

Qubit connectivity of some representative quantum computing systems



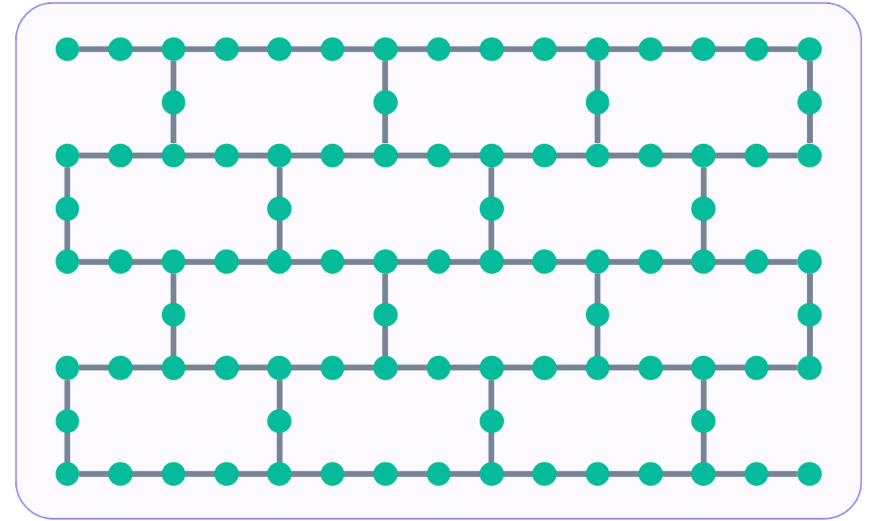
(a) 2D grid

Example: Google Sycamore



(b) Octagonal

Example: Rigetti



(c) Heavy-hex

Example: IBM Falcon

The hardware structure exhibits translation symmetry, rotation symmetry, inversion symmetry...

Symmetry-based quantum circuit mapping: algorithm

We have shown that, in many practical cases, this algorithm has a time complexity of $O(n)$ with n the number of qubits in the hardware, which is optimal for the subgraph matching problem.

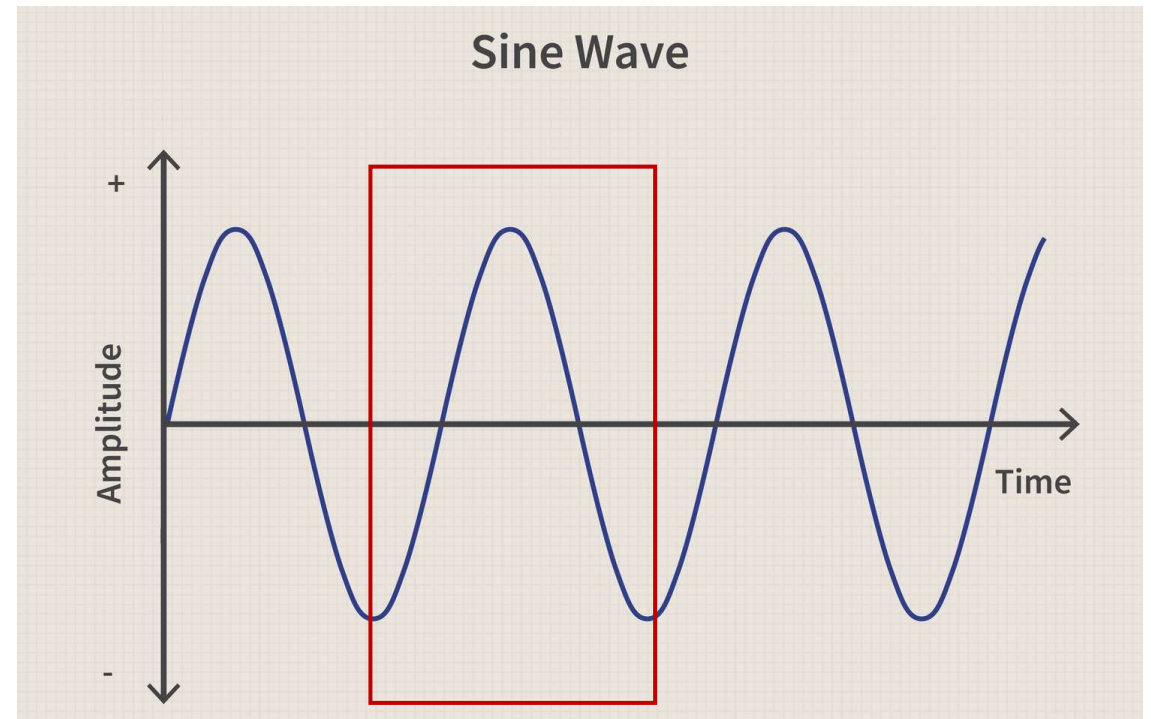
ALGORITHM 1. Symmetry-based subgraph matching

Input : A pattern graph G , a target graph T , a group of automorphisms F of the target graph and the associated generating set S .

Output: All subgraph isomorphisms of G in T .

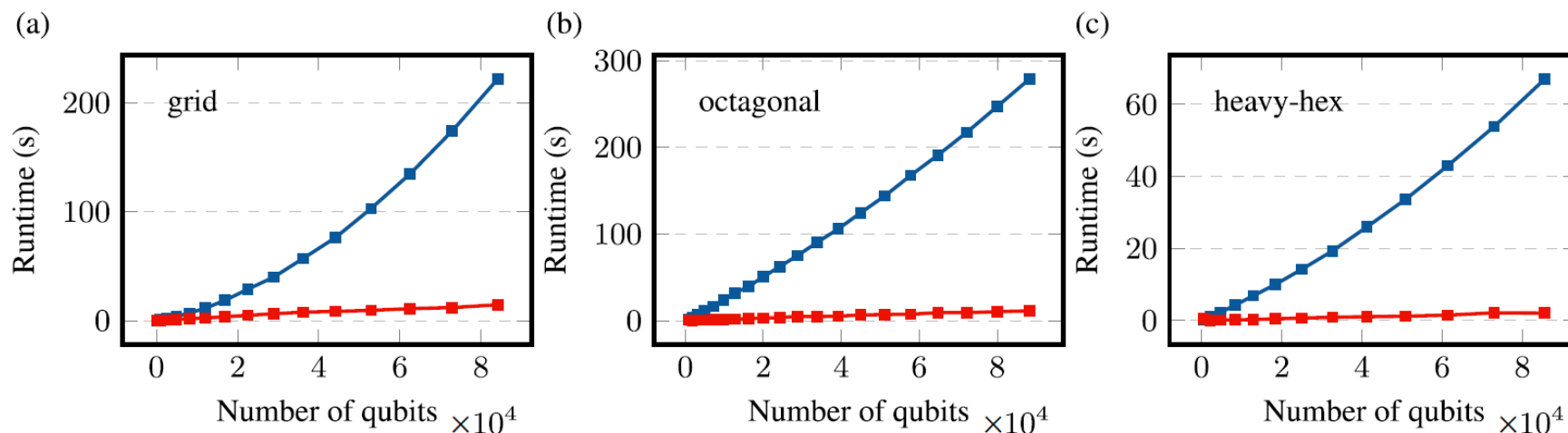
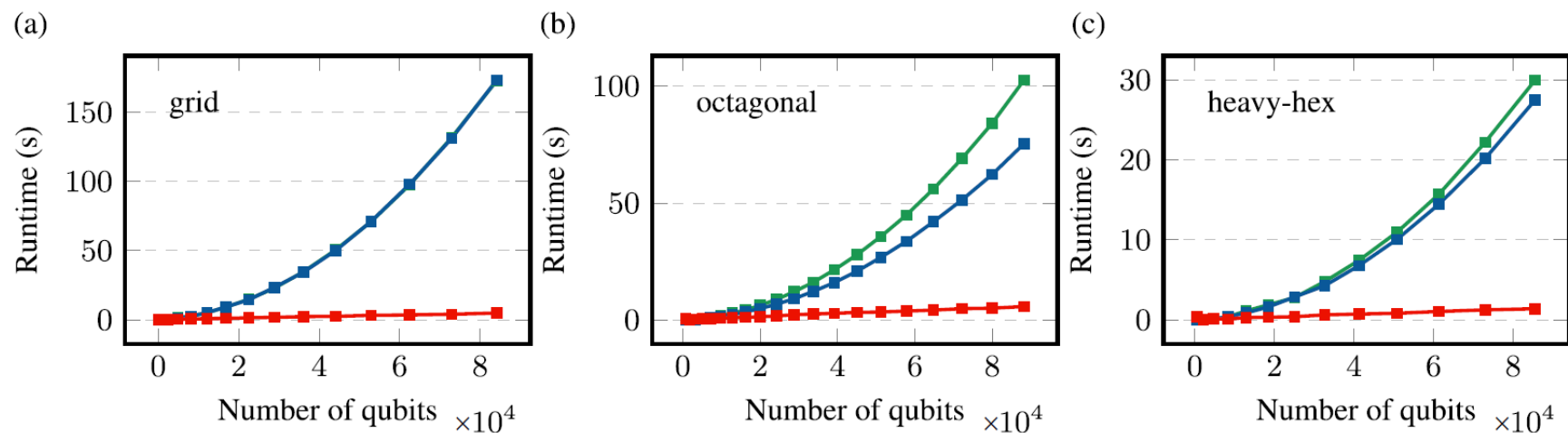
- 1 Let r be the radius of the pattern graph G ;
- 2 Let $N_T^r(S)$ be the r -th order neighborhood of S ;
- 3 Let R be the induced subgraph of $N_T^r(S)$ in T ;
- 4 Obtain the set of all isomorphic graphs of G within R and denote this set as H_0 ;
- 5 Let H be an empty list;
- 6 **for** $G' \in H_0$ **do**
- 7 Let $M = \{\tilde{f}(G') : f \in F, \tilde{f}(G') \subseteq T\}$;
- 8 Append M to H ;
- 9 **end**
- 10 Return H ;

Algorithm	Time complexity
VF2	$O(n^2) \sim O(n! n)$
SBSM (this work)	$O(n)$



Finding all the maxima = find all maxima in one period

Numerical comparison



IBM qiskit

Dynamic quantum circuit has great advantage in reducing the # qubits

Symmetry has great advantage in reducing the complexity of circuit compilation

Thanks for your attention!

2310.11021 & PRApplied 22, 024029

for more details

I am hiring postdocs, PhDs, research assistants...

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